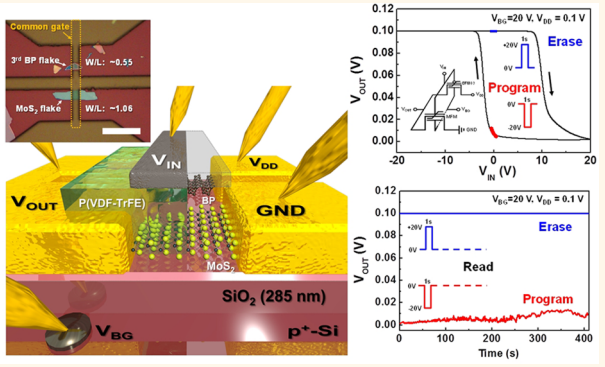
Nonvolatile Ferroelectric Memory Circuit Using Black Phosphorus Nanosheet-Based Field-Effect Transistors with P(VDF-TrFE) Polymer

Young Tack Lee,[†,§] Hyeokjae Kwon,[‡,§] Jin Sung Kim,[‡] Hong-Hee Kim,[⊥] Yun Jae Lee,[†] Jung Ah Lim,[†] Yong-Won Song,[†] Yeonjin Yi,[‡] Won-Kook Choi,[*,⊥,∥] Do Kyung Hwang,[*,†,∥] and Seongil Im[*,‡]

[†]Center of Opto-Electronic Materials and Devices, Post-Silicon Semiconductor Institute, Korea Institute of Science and Technology (KIST), Seoul 136-791, Korea, [‡]Institute of Physics and Applied Physics, Yonsei University, Seoul 120-749, Korea, [⊥]Materials and Life Science Research Division, Korea Institute of Science and Technology (KIST), Seoul 136-791, Korea, and [∥]Department of Nanomaterials and Nano Science, Korea University of Science and Technology (KUST), Daejun 305-350, Korea. [§]Y. T. Lee and H. Kwon contributed equally.

ABSTRACT Two-dimensional van der Waals (2D vdWs) materials are a class of new materials that can provide important resources for future electronics and materials sciences due to their unique physical properties. Among 2D vdWs materials, black phosphorus (BP) has exhibited significant potential for use in electronic and optoelectronic applications because of its allotropic properties, high mobility, and direct and narrow band gap. Here, we demonstrate a few-layered BP-based nonvolatile memory transistor with a poly(vinylidenefluoride-trifluoroethylene) (P(VDF-TrFE)) ferroelectric top gate insulator. Experiments showed that our BP-based ferroelectric transistors operate satisfactorily at room temperature in ambient air and exhibit a clear memory window. Unlike conventional ambipolar BP transistors, our ferroelectric transistors showed only p-type characteristics due to the carbon—fluorine (C—F) dipole effect of the P(VDF-TrFE) layer, as well as the highest linear mobility value of 1159 $cm^2 V^{-1} s^{-1}$ with a 10^3 on/off current ratio. For more advanced memory applications beyond unit memory devices, we implemented two memory inverter circuits, a resistive-load inverter circuit and a complementary inverter circuit, combined with an n-type molybdenum disulfide (MoS_2) nanosheet. Our memory inverter circuits displayed a clear memory window of 15 V and memory output voltage efficiency of 95%.



KEYWORDS: black phosphorus (BP) · MoS_2 · 2D nanosheet transistor · P(VDF-TrFE) · ferroelectric memory CMOS · dual-gate transistor

Since the discovery of graphene,[1−6] two-dimensional (2D) van der Waals (vdWs) materials have become an active area of research because of their unique physical properties. Fundamental studies have been conducted on the material properties of 2D vdWs, and electronic and optoelectronic applications for these have been developed with unprecedented speed. Like graphene, semiconductor layers composed of 2D vdWs, with a high-quality, single-crystal structure, can be obtained in general by facile mechanical exfoliation. Of the many 2D vdWs materials, transition metal dichalcogenide (TMD) semiconductors are regarded as promising alternatives to graphene as high off current level (little on/off current ratio). Molybdenum disulfide (MoS_2)[7−14] and tungsten diselenide (WSe_2)[15−22] are the representative n-type and p-type (or p-type dominant ambipolar) TMD semiconductors, respectively. Many research groups have demonstrated developed monolayer MoS_2 nanosheet transistors that exhibit satisfactory carrier mobility values with high on/off current ratios, unlike in the case of graphene transistor devices.[7−11] WSe_2 has been extensively studied, and several electronic/optoelectronic applications of it have been proposed.[15,18−21] Hence, the nanoscience and nanotechnology based on

* Address correspondence to (W.-K. Choi) wkchoi@kist.re.kr, (D. K. Hwang) dkhwang@kist.re.kr, (S. Im) semicon@yonsei.ac.kr.

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these two representative TMD materials are gradually maturing.

On the other hand, a newly discovered 2D vdWs material,[23−33] called black phosphorus (BP), has generated considerable scientific and technological interest in the research community because of its unique properties: it is an allotropic material (puckered honeycomb structure)[23,24] that is an ambipolar semiconductor[25−28] with high mobility (~1000 $cm^2 V^{-1} s^{-1}$)[23] and a narrow and direct band gap (~0.3 eV, >10 layers).[24−26] For these reasons, 2D BP has considerable potential for electronic and optoelectronic applications. This is evidenced by recent research on field-effect transistors (FETs),[23,24,26−28] diodes,[29,30] and photodetectors[31,32] involving few-layered BP flakes. However, more advanced devices beyond basic unit ones, such as a logic circuit or nonvolatile memory, have not been comprehensively explored.[24]

Here, we demonstrated the first few-layered, BP-based nonvolatile memory FETs using the ferroelectric copolymer poly(vinylidenefluoride-trifluoroethylene) [P(VDF-TrFE)] as the top gate insulator (GI) layer, with the aim of developing 2D vdW material-based memory logic circuit applications, such as a resistive-load inverter or complementary metal−oxide−semiconductor (CMOS) inverter circuits. According to the relevant past literature, few-layered BPs with thickness values in the region of 5−10 nm show higher field-effect mobility.[23,24] Therefore, we used few-layered BP as the channel layer, instead of monolayered or bilayered BP, for our memory devices. Our BP ferroelectric FETs (FeFETs) exhibited a clear memory window of 15 V and a highest linear mobility value of 1159 $cm^2 V^{-1} s^{-1}$ with a 10^3 on/off current ratio at room temperature in ambient air. Unlike conventional ambipolar BP transistors, our FeFETs showed only p-type characteristics because the abundance of carbon−fluorine (C−F) dipoles inside P(VDF-TrFE) suppressed n-type characteristics.[34−38] In order to explore advanced memory applications beyond unit memory devices, we implemented two kinds of memory inverter circuits: a resistive-load inverter circuit and a CMOS inverter circuit combined with n-type MoS_2. Both memory inverters directly converted analog signals (current) to digital signals (voltage) and displayed a clear memory window of 15 V and memory output voltage efficiency values of 95%.

RESULTS AND DISCUSSION

We prepared a clean, 285 nm thick SiO_2/p^+-Si wafer as a substrate for our BP FETs for thickness estimation and basic FET characterization prior to fabricating the top gate FeFETs. Figure 1a−d show optical microscopic (OM) images of the first (1st) and second (2nd) BP nanosheets and of the as-fabricated FETs (each scale bar was 30 μm long). We used a polydimethylsiloxane (PDMS) stamp to exfoliate and transfer the BP nanosheets onto the p^+-Si substrate. In order to make ohmic contact with the BP nanosheets, Au/Ti (50 nm/25 nm) source and drain (S/D) electrodes were formed by

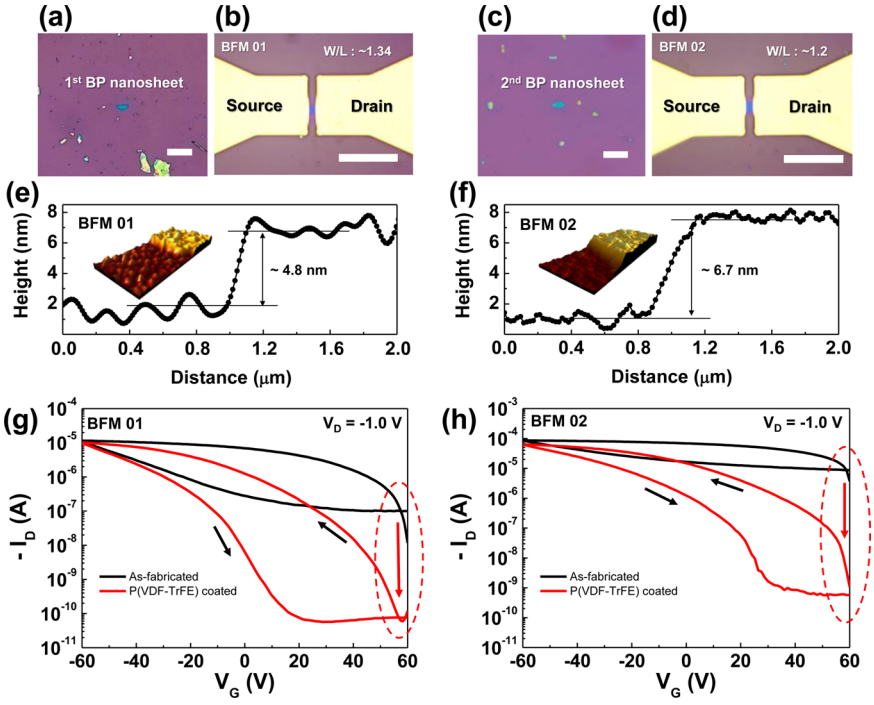

Figure 1. OM images from exfoliated BP nanoflakes on an Si substrate and as-fabricated FETs, (a and b) BFM 01 (*W*/*L* = 1.34) and (c and d) BFM 02 (*W*/*L* = 1.2). AFM step-height profiles and the inset surface topographic images of the (e) BFM 01 and (f) BFM 02. (g and h) I_D *vs* V_G transfer characteristics of our BFM 01 and BFM 02. The black and red lines indicate the electrical properties of the as-fabricated and P(VDF-TrFE)-coated BP transistors, respectively.

photolithography, and a channel length of ~5 μm was used. We will refer to our developed BP ferroelectric memory as "BFM No. (sample number)". According to the step-height profiles obtained from an atomic force microscope (AFM) as shown in Figure 1e and f, our BP nanosheets for the BFM 01 and BFM 02 devices were confirmed to be ~4.8 nm and ~6.7 nm thick, respectively, whereas the insets show the 3D topographic images of each device. In order to confirm the material properties of our BP nanosheets, we conducted X-ray diffraction (XRD; ATX-G, Rigaku; Cu Kα = 0.154 nm) and scanning electron microscopy (SEM)/energy dispersive X-ray (EDX) (Inspect F50, FEI) measurements (see Figure S1 in the Supporting Information). All static electrical measurements of our devices, such as I_D *vs* V_G transfer, voltage memory hysteresis characteristics (VMHCs), and retention properties, were measured using a 4155C semiconductor parameter analyzer and an Agilent 4284A in the dark at room temperature (air ambient).

Figure 1g and h show the transfer characteristics of BFM 01 and BFM 02 under the bottom gate (BG) operation, respectively. The black and red lines indicate the results of the as-fabricated and P(VDF-TrFE) (220 nm)-coated devices, respectively (see Figure S2 for device schematic views in the Supporting Information). Both as-fabricated BFM devices showed significant hysteresis (counterclockwise) and low on/off drain current (I_{on}/I_{off}) ratios of ~10^2 at a drain voltage (V_D) of −1.0 V. However, following P(VDF-TrFE) layer deposition, in order to fabricate the top gate FeFET memory, we significantly increased the I_{on}/I_{off} ratios to ~10^5 (see the red dashed circles in Figure 1g and h). Such improvement can be correlated with the electric dipole effect of the carbon−fluorine (C−F) bonds in the end groups of the P(VDF-TrFE). In research on organic semiconductors, several studies have reported dipole effects of fluorine functional groups that can modulate charge carrier density on channel layers.[34−38] We believe that the abundance of C−F dipoles inside P(VDF-TrFE) induces high positive charge densities (enhancing p-type characteristics) while preventing charge injection for the electron (hence suppressing n-type characteristics) from the S/D electrodes. In our previous study, similar phenomena were observed in WSe_2 and MoS_2 TMD materials.[38] Linear mobility (μ_{lin}) is plotted for each transfer curve (Figure S3 in the Supporting Information) and is calculated by the following equations:

$$g_m(V_G) = \frac{\partial I_D}{\partial V_G} \quad (1)$$

$$\mu_{lin}(V_G) = \frac{g_m(V_G)}{C_{ox}V_D}\left(\frac{L}{W}\right) \quad (2)$$

where $g_m(V_G)$ and C_{ox}, respectively, represent gate voltage (V_G)-dependent transconductance and capacitance of the GI layer. The maximum μ_{lin} values of BFM 01 and BFM 02 under the BG operation with the P(VDF-TrFE) top layer were 297 and 1298 $cm^2\ V^{-1}\ s^{-1}$, respectively.

Figure 2a shows a 3D schematic cross-sectional view of our BP top gate FeFET. Al top gate electrode layers were deposited using thermal evaporation and patterned through a lift-off process. The 220 nm thick P(VDF-TrFE) ferroelectric polymer insulator yielded a coercive electric field of ~0.55 MV cm^{-1} and coercive voltage of ~11 V (see Figure S4 for the general remnant charge density-applied electric field (P_r−E) and the capacitance−voltage (C−V) curves in the Supporting Information). Figure 2b and c show the operating mechanism of our BP FeFET under coercive V_G pulses of ∓20 V. The BP FeFETs were in the ON state (accumulation of holes, program state) following a negative pulse for 1 s but were in the OFF state (depletion of holes) after a positive pulse for 1 s. Figure 2d and e exhibit memory hysteresis loops at several V_G sweep ranges under a V_D of −0.1 V. When small V_G sweep ranges of ±5 and 10 V were taken, neither BFM 01 nor BFM 02 exhibited memory hysteresis windows. At V_G sweep ranges of more than ±15 V, memory windows were clearly observed, which phenomenon can be related to the coercive voltage of P(VDF-TrFE) ferroelectric polymer (~11 V). When V_G higher than the coercive voltage was applied to P(VDF-TrFE), ferroelectric dipoles in the polymer could be aligned (electrical polarization), resulting in the generation of memory windows. The memory window became larger given higher V_G sweeps of ±20 V. It is worth noting that the direction of the memory hysteresis loop was opposite that in the transfer curves driven by the BG (Figure 1g and 1h). (Note here that the hysteresis of BP FETs driven by the BG was volatile hysteresis, which cannot be used for nonvolatile memory devices.) Our plots of linear mobility (μ_{lin}) against V_G values of our BFM devices are shown in Figure 2f and g. The C_{ox} value of the P(VDF-TrFE) GI ($C_{ox,P(VDF-TrFE)}$) was not constant but V_G dependent (see Figure S4a for the $C_{ox,\ P(VFD-TrFE)}$ plot as a function of V_G in the Supporting Information). Taking account of V_G-dependent $C_{ox,\ P(VFD-TrFE)}$, the maximum μ_{lin} values of BFM 01 and BFM 02 were estimated to be 131 and 574 $cm^2\ V^{-1}\ s^{-1}$ at a V_G sweep of ±20 V with a V_D of −0.1 V.

On the basis of the above understanding of our BP layers with a ferroelectric GI, we attempted three approaches to nonvolatile memory devices for more practical and advanced applications. The first involved a basic FeFET memory device (using BFM 01), the second approach consisted of forming a resistive-load inverter ferroelectric memory circuit (using BFM 02), and the third concerned a CMOS inverter memory circuit (using BFM 03) combined with an n-type MoS_2 ferroelectric memory transistor on the same substrate.

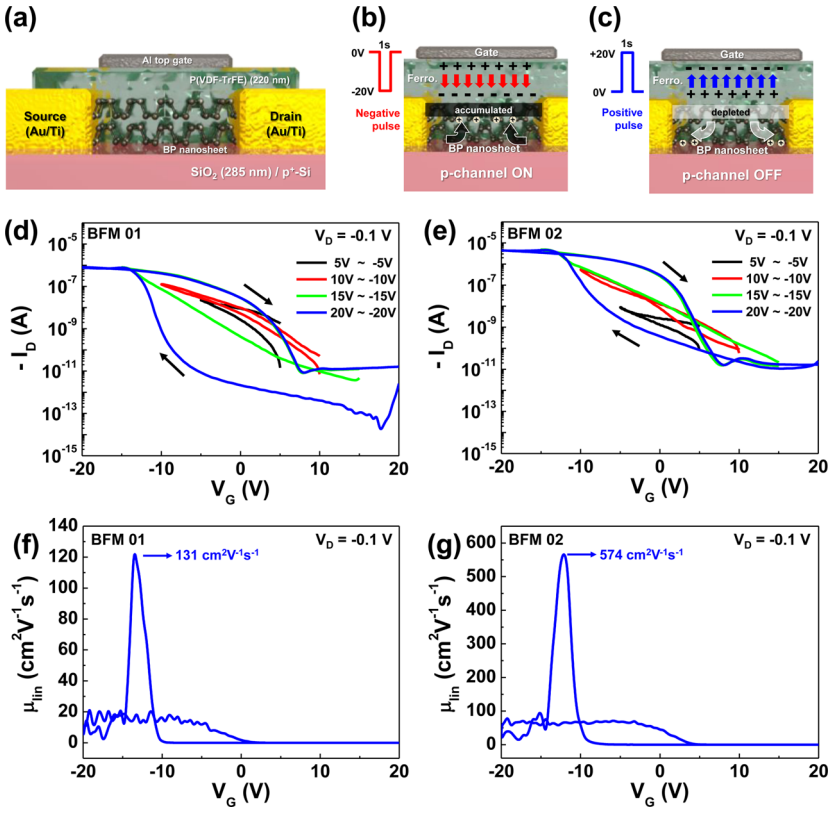

Figure 2. (a) 3D cross-sectional schematic view of BFM (BP FeFET). Schematic illustrations of BFM mechanisms for program and erase states. (b) p-Channel ON (hole accumulation) after a −20 V pulse and (c) p-channel OFF (hole depletion) after a +20 V pulse, respectively (arrows indicate dipole direction). (d and e) I_D *vs* V_G memory hysteresis loops of BFM 01 and BFM 02 at several V_G sweep ranges under a V_D of −0.1 V. (f and g) Linear mobility *vs* V_G plots of the BFM 01 and BFM 02 at a V_G sweep of ±20 V at a V_D of −0.1 V, respectively.

After long-range V_G double sweeps (from +20 V to −20 V) for memory hysteresis, we applied a V_G pulse of ∓20 V for 1 s to set program and erase states on our BP FeFET (BFM 01), followed immediately by a short-range V_G sweep of 0.5 V to −0.5 V. Two distinct states of program (PRO) (red line), following the −20 V pulse, and erase (ER) (blue line), following the +20 V pulse with a high PRO/ER drain current (I_{PRO}/I_{ER}) ratio of ∼10^4, were clearly observed. These were superimposed on long-range memory hysteresis curves at a V_D of −0.1 V, as shown in Figure 3a. The memory retention property test was also carried out, as shown in Figure 3b. The retention properties of BP FeFET were measured under a V_D of −0.1 V and floating V_G conditions following the PRO (−20 V) and ER (+20 V) V_G pulses for 1 s. The two distinctive states (PRO and ER) were maintained for 1000 s without serious I_{PRO}/I_{ER} ratio degradation.

Following the basic memory property characterizations, we extended our study of BP FeFETs to memory inverter circuit applications and first implemented a resistive-load inverter with the BFM 02 device. The basic memory properties of the BFM 02 device for the PRO and ER states following the V_G pulses of ∓20 V for 1 s were measured, as shown in Figure 3c. The memory performance of BFM 02 was quite similar to that of BFM 01 and yielded an I_{PRO}/I_{ER} ratio of ∼10^3. For successful inverter memory circuit operation, an external resistor (R_{EXT}) of 10 MΩ was chosen in light of V_G-dependent resistance values of the BFM 02 device, which were ∼3 kΩ at the ON state and ∼1 GΩ at the OFF state (see Figure S5 in the Supporting Information). Figure 3d shows the schematic view of our ferroelectric resistive-load inverter memory circuit consisting of our BFM 02 and an R_{EXT} of 10 MΩ. According to the VMHC of our ferroelectric inverter memory in Figure 3e, the memory window was ∼13 V at a supply voltage (V_{DD}) of −0.1 V, which was consistent with the result obtained from transfer characteristics in Figure 3c. The input voltage (V_{IN}) pulses of ∓20 V for 1 s could set certain PRO and ER output voltage (V_{OUT}) memory signals, as shown in the short-range V_{IN} sweep of Figure 3e. The memory V_{OUT} efficiency of our ferroelectric inverter memory for the PRO and ER states, defined as ($V_{OUT,\ PRO} - V_{OUT,ER}$)/$V_{DD}$ × 100 (%), was estimated to be ∼88% at a V_{DD} of −0.1 V. Figure 3f shows V_{OUT} retention properties following PRO (−20 V) and ER (20 V) for a V_{IN} pulse of 1 s, which were also maintained satisfactorily for 1000 s under a constant V_{DD} of −0.1 V and the floating V_{IN} condition. It is worth noting that the P(VDF-TrFE) top layer can retard the degradation process, although it is not an excellent barrier for the passivation of BP-based devices. The BFM02 device was exposed to ambient air

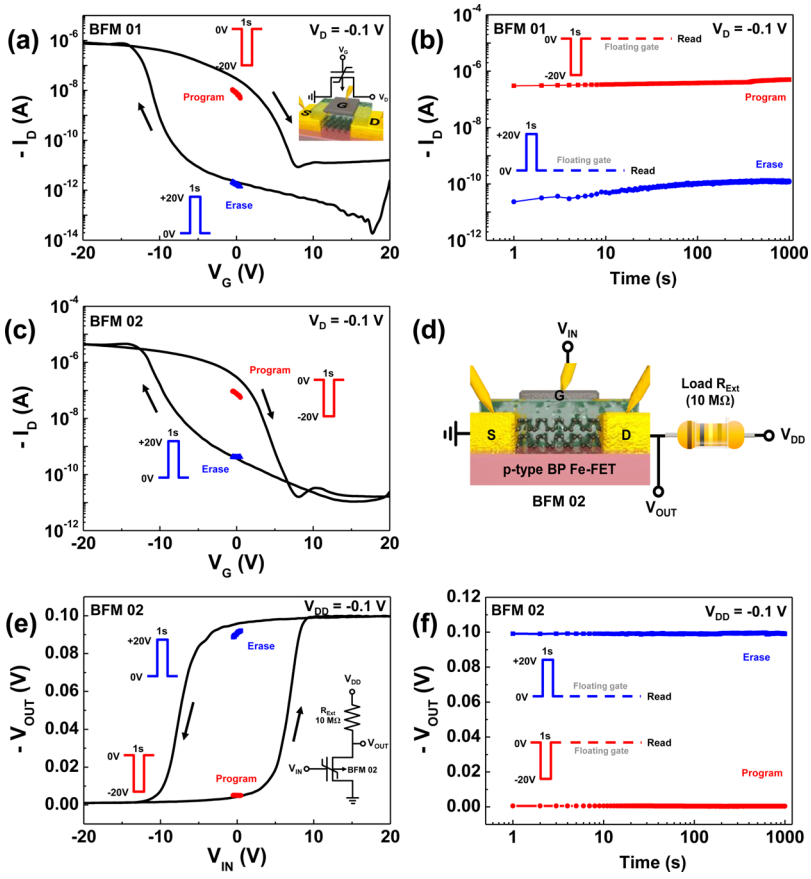

Figure 3. (a) I_D *vs* V_G memory hysteresis curves of BFM 01 at a small V_G sweep range of 0.5 ≤ V_G ≤ −0.5 V and a V_D of −0.1 V, obtained after PRO (red line, −20 V for 1 s) and ER (blue line, 20 V for 1 s) pulses. Inset illustration shows a schematic view of the 3D device and a circuit diagram of our BFM 01. (b) Retention I_D properties of PRO and ER states recorded under a V_D of −0.1 V. (c) I_D *vs* V_G memory hysteresis curves of BFM 02, and recordable PRO (red line) and ER (blue line) states for a short-range V_G sweep at V_D of −0.1 V. (d) 3D schematic view of the ferroelectric resistive-load inverter memory circuit consisting of BFM 02 and external resistor (10 MΩ). (e) VMHCs of the ferroelectric inverter memory circuit and the recordable PRO (red line) and ER (blue line) states (voltage signal) for a short-range V_G sweep at a V_D of −0.1 V. Inset shows the circuit diagram. (f) Retention V_{OUT} properties for PRO and ER states recorded under a V_{DD} of −0.1 V.

for 1 week and remeasured. Interestingly, we found an aging effect: the BP FeFET exhibited somewhat enhanced memory properties along with an enhanced field-effect mobility value from 574 $cm^2\ V^{-1}\ s^{-1}$ to 1562 $cm^2\ V^{-1}\ s^{-1}$ (see Figure S.6 in the Supporting Information). However, we may need further research to understand this effect in depth.

Finally, we built a ferroelectric CMOS (FeCMOS) memory circuit consisting of BP FeFET (p-type) and MoS_2 FeFET (n-type). Figure 4a shows an OM image of our FeCMOS memory device comprising the third (3rd) few-layered BP (BFM 03) (top side, W/L = 0.55) and the MoS_2 (bottom side, W/L = 1.06) flakes. (Hereafter, we refer to our MoS_2 ferroelectric memory as MFM 01, which is analogous to BFM 03 with BP.) Based on an AFM step-height analysis as shown in Figure 4b, the thickness values of the BP for BFM 03 and the MoS_2 for MFM 01 were estimated to be ∼7.2 nm and ∼12.5 nm, respectively (note: the insets show the 3D topographic images of each flake). Because BP typically has higher mobility (higher drain current level) than MoS_2, we selected a thicker MoS_2 flake in order to match the I_D levels between the BFM and MFM devices. Nonetheless, there was a significant difference in I_D levels between the BFM and MFM devices, whereas the I_{OFF} of the BFM 03 transistor was similar to the I_{ON} of the MFM 01 transistor. This was also attributed to the C−F dipoles of the P(VDF-TrFE) layer, which suppressed the n-type characteristics of MoS_2 while enhancing the p-type characteristics of BP. In order to counteract the effects of the C−F dipole, we connected an additional electrode to the BG (p^+-Si), which enabled dual-gate (DG) transistor operation.[39,40] Figure 4c shows the 3D schematic cross-sectional view of our dual-gate FeCMOS memory circuit, composed of BFM 03 and MFM 01, on the same substrate. The memory window hysteresis curves (I_D *vs* V_G) of BFM 03 (solid symbol) and MFM 01 (hollow symbol), driven by the DG operation of the top gate voltage (V_{TG}) sweep at a fixed bottom gate voltage (V_{BG}) of 0 to 20 V with five-volt steps (V_D = ± 0.1 V), are shown in Figure 4d. In the case of the BFM 03 transistor, the fixed positive V_{BG} induced a reduction in both the I_{ON} and I_{OFF} along with a negative threshold voltage (V_{th}) shift, but the overall

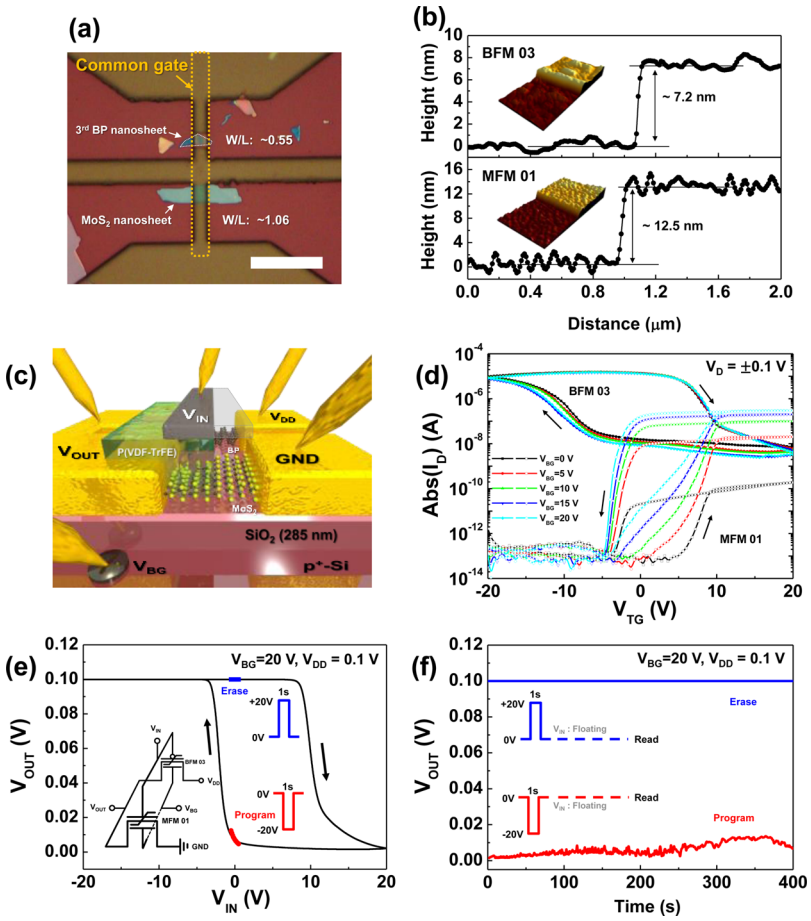

Figure 4. (a) OM image of the dual-gate FeCMOS consisting of the p-type BFM 03 (W/L = 0.55) and n-type MFM 01 (W/L = 1.06) on the same p+-Si substrate. (b) AFM step-height profiles and inset surface topographic images of BFM 03 (top) and MFM 02 (bottom). (c) 3D schematic view of the dual-gate FeCMOS composed of 2D vdW active channel (BP and MoS_2). (d) I_D *vs* V_G memory hysteresis curves of BFM 03 (solid symbol) and the MFM 01 (hollow symbol) obtained by dual-gate driving at a fixed V_{BG} of 0−20 V (5 V steps). (e) VMHCs of the dual-gate FeCMOS with fixed V_{BG} of 20 V and recordable PRO (red line) and ER (blue line) states for a short-range V_{IN} sweep at a V_{DD} of 0.1 V. Inset figure shows the circuit diagram of our dual-gate FeCMOS. (f) Retention V_{OUT} properties for PRO and ER states recorded under a V_{DD} of 0.1 V and a fixed V_{BG} of 20 V.

changes were not significant. For comparison, we measured the memory transfer characteristics of BFM 03 driven by a single-top-gate operation (V_{TG} sweep) and a DG operation. Although the maximum μ_{lin} value of 1159 $cm^2\ V^{-1}\ s^{-1}$ obtained from a single V_{TG} sweep was slightly higher than that of 1016 $cm^2\ V^{-1}\ s^{-1}$ obtained from the V_{TG} and V_{BG} sweep, the effect of the value of V_{BG} on the performance of the BFM 03 device was not critical. More details regarding the BFM 03 transistor under TG and DG operations are shown in Figure S7 in the Supporting Information. On the contrary, for the MFM 01 transistor, V_{BG} led to significant changes in the I_{ON} level and the V_{th} shift: a higher positive value of V_{BG} induced larger I_{ON} along with a negative V_{th} shift. At V_{BG} over 10 V, the I_{ON} of the MFM 01 transistor surpassed the I_{OFF} of the BFM 03 transistor, which facilitated CMOS memory circuit operation.

As expected, the voltage memory hysteresis of our dual-gate FeCMOS device became apparent at a V_{BG} of 10 V, but clearer VMHC curves with a ∼12 V memory window were obtained at V_{BG} values of 15 and 20 V (see Figure S8 of the VMHC curves, obtained from our FeCMOS circuit at several fixed values of V_{BG} in the Supporting Information). We chose the best condition (V_{BG} = 20 V) and attempted to measure the memory-based properties of our FeCMOS circuit following a short V_{IN} pulse signal of ∓20 V. Figure 4e shows the VMHC curve and clear PRO/ER states with a memory V_{OUT} efficiency of ∼95% achieved at a fixed V_{BG} of 20 V and V_{DD} of 0.1 V through a short-range V_{IN} sweep following V_{IN} pulses of 1 s (note: the inset is the circuit diagram). We also attempted to measure the retention properties of the FeCMOS circuit under a floating V_{IN} with fixed V_{BG} (= 20 V) and a constant V_{DD} of 0.1 V. Figure 4f shows the retention properties of the two distinctive $V_{OUT,PRO}$ and $V_{OUT,ER}$ states, which were maintained and recorded for ∼400 s with the memory V_{OUT} efficiency of ∼95%. For a brief summary of all properties of our BP nanosheet-based ferroelectric memory devices, see Table 1, where performance parameters such as maximum

TABLE 1. Electrical and Memory-Related Performance Parameters of BFM 01, 02, and 03 FeFETs

sample name	thickness (nm)	*W*/*L* ratio	max μ_{lin}[a] ($cm^2\ V^{-1}\ s^{-1}$)	I_{ON}/I_{OFF} ratio	I_{ON}(A) @ $V_D = -0.1$ V	SS[b] (V dec^{-1})	memory window (V)	memory V_{OUT} efficiency (%)
BFM 01	~4.8	~1.34	131	$\sim 1.45 \times 10^6$	$\sim 7.6 \times 10^{-7}$	~0.9	14.6	
BFM 02	~6.7	~1.2	574	$\sim 2.6 \times 10^5$	$\sim 4.4 \times 10^{-6}$	~1.4	11.4	~88
BFM 03	~−7.2	~0.55	1159	$\sim 1.3 \times 10^3$	$\sim 9.9 \times 10^{-6}$	~3.3	15.6	~95

[a] Maximum linear mobility. [b] Subthreshold voltage.

μ_{lin}, I_{ON}/I_{OFF} ratio, subthreshold slope (SS), and memory window are listed.

CONCLUSIONS

In conclusion, we developed few-layered, BP nanosheet-based ferroelectric memory transistor devices and inverter memory circuits using a P(VDF-TrFE) polymer top gate dielectric. Unlike conventional ambipolar BP transistors, our FeFETs showed only p-type characteristics due to the C−F dipole effect of the P(VDF-TrFE) layer. Our BP FeFETs exhibited high linear mobility values (maximum 1159 $cm^2\ V^{-1}\ s^{-1}$), high on/off I_D ratios of $\sim 10^5$, and satisfactory memory properties with a ~12 V window. Moreover, we successfully implemented two kinds of memory inverter circuits to directly convert analog signals (current) to digital signals (voltage). Our two memory inverter circuits, the resistive-load inverter circuit and the complementary inverter circuit combined with n-type MoS_2, displayed a clear memory window of 15 V and a high memory output voltage efficiency of ~95%. We thus believe that the results of our BP-based nonvolatile ferroelectric memory transistors and inverter circuits exhibit promising perspectives for the future of 2D nanoelectronics for more advanced electronic applications.

METHODS

Ferroelectric P(VDF-TrFE) Gate Insulator Layer. To fabricate a ferroelectric GI layer, a P(VDF-TrFE) 70:30 mol % copolymer powder was first dissolved in a dimethylformamide (DMF) solvent at a 6 wt % ratio. A 220 nm thick GI film was then formed through spin-casting and thermal annealing. The thermal treatment was performed in two steps, at 70 °C for 5 min and 140 °C for 1 h. Because both DMF and P(VDF-TrFE) are very sensitive to humidity, all processes were carried out in a nitrogen-filled glovebox at very low humidity.

Conflict of Interest: The authors declare no competing financial interest.

Supporting Information Available: The Supporting Information is available free of charge on the ACS Publications website at DOI: 10.1021/acsnano.5b04592.

XRD and SEM/EDX of BP flakes, device schematics of bottom-gate BP FETs, linear mobility *vs* V_G plots, electrical properties of ferroelectric P(VDF-TrFE) GI layer, V_G-R_{ch} plot of the BFM 02, aging effect of the BFM 02, dual gate sweep of the BFM 03 and dual-gate effect of FeCMOS (PDF)

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